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Memory 550 includes a FIFO buffer 710, a write pointer register 720, and a .... Byte packer 1050 may operate upon the packets to remove intrapacket gaps. ...

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final ES, a byte-packer, and a NAL unit encoder as illustrated. in Fig.3. .... subsequent pipe register are generated based on the state. As ...

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register and the mask register to overwrite selectively ... First, a hardware byte packer for the Boot. ROM is not necessary, as the packing can be done by ...

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byte packer buffer. GR1..GR6. 16. general registers 1 to 6. XR. 16. index register (GRI-99 only). BOV. 1. bus overflow (MSR&lt;15&gt;) ...

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The bus address register 312 is driven by the address in on line 301. The ..... Data from the byte packer 420 is supplied to the packing cell buffer 423. ...

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a byte packer configured to remove the gaps from the multiplexed packets. ... a write pointer register configured to store a plurality of the write stream ...

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Method and system for efficiently using buffer space invention

SDE 319 includes a byte packer function that takes unaligned or less than 8 ... [0054]

Register interface 312 provides host 100 access to plural system 102 ...

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return the value of the incomplete word in the byte-packer. Reads to this register will not affect the state of the receive FIFO, including the head and ...

[ftp://ftp.netbsd.org/pub/NetBSD/misc/dec-docs/TclA\\_spec1.0.ps.gz](ftp://ftp.netbsd.org/pub/NetBSD/misc/dec-docs/TclA_spec1.0.ps.gz) - [Similar pages](#)  
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... 1st cycle delay \*/ uint32 packer; /\* byte-packer holding reg \*/ ... base page fence \*/ /\* Map violation register \*/ #define MVI\_V\_RPR 15 /\* must be ...

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A system with a 1-MHz 3-register 8-bit processor and 64 kilobytes of ..... to have a sequence cruncher on top of an RLE (or equal-byte) packer or linker. ...

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This register accepts information directly from the Transmit FIFO, the Transmit Input Register, the 10/8 Byte-Packer, or, from the Transmit Control State ...

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register is loaded with a value between 0 and 255 that reflects the temperature differential ..... 8-bit to 1-byte Packer Symbol. Enables you to construct ...

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Although it is possible for programs to accidentally reconfigure the SCPU, it is awfully unlikely, since the enable register, which switches the hardware ...

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Ethernet Plug-and-play Register

Configuration Sequence . . . . . 5–8. 5–4. Ethernet Plug-and-play Register Initial Values .

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FIFOs) or as a pipeline register extender. The FIFO configura- ..... to be driven as a pipeline register and RXEN is assumed to be driven by a ...

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US Pat. 6952738 - Juniper Networks, Inc.

Byte packer 540 may include conventional byte packing mechanisms that process ... Memory

550 includes a FIFO buffer 710, a write pointer register 720, ...

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